APPLICATION NO.10/707756

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CLMPTO

1. A method for fabricating a bipolar transistor with a raised extrinsic base, an emitter and a collector, the method comprising the steps of:

a) providing an intrinsic base layer;

b) forming a first insulator layer on a portion of the intrinsic base layer;

c) forming a raised extrinsic base layer on the first insulator layer and the intrinsic base layer;

d) forming a second insulator layer on the extrinsic base layer;

e) providing an emitter opening by selectively removing portions of the extrinsic base layer and the second insulator layer to expose a portion of the first insulator layer;

f) forming a spacer along a sidewall of the emitter opening;

g) selectively removing the first insulator layer;

h) forming a conductor in a space vacated by the first insulator layer;

i) converting the conductor within the emitter opening to a third insulator such that the third insulator extends under at least a portion of the spacer; and

j) forming the emitter.

2. The method of claim 1, wherein the selectively removing step includes etching to remove the first insulator layer from the emitter opening, under the spacer and under a portion of the extrinsic base layer.

3. The method of claim 2, further comprising the step of removing the third insulator within the emitter opening to the intrinsic base layer, leaving a remaining portion of the third insulator under the at least a portion of the spacer.

4. The method of claim 1, wherein the extrinsic base layer is non-planar.

5. The method of claim 1, wherein the raised extrinsic base layer comprises one of: a polysilicon and single crystalline silicon.

6. The method of claim 1, wherein the conductor comprises single crystalline silicon.

7. The method of claim 1, wherein the emitter forming step includes depositing, patterning and etching a polysilicon.

CLAIMS 8-13 (CANCELLED)

14. A method for fabricating a bipolar transistor with a raised extrinsic base, an emitter and a collector, the method comprising the steps of:

a) providing a landing pad positioned between an in-

trinsic base layer and an extrinsic base layer;

b) providing an emitter opening by selectively removing portions of the extrinsic base layer to expose a portion of the landing pad;

c) forming a spacer along a sidewall of the emitter opening;

d) selectively removing the landing pad from the emitter opening, under the spacer and under a portion of the extrinsic base layer;

e) forming a conductor in a space vacated by the landing pad;

f) converting the conductor in the emitter opening and at least a portion under the spacer to an insulator;

g) removing the insulator from within the emitter opening; and

h) forming the emitter.

15. The method of claim 14, wherein the converting step includes oxidizing the conductor to form an oxide insulator within the emitter opening such that the oxide insulator extends under at least a portion of the spacer but not into the extrinsic base layer.

16. The method of claim 14, wherein the emitter forming step includes depositing, patterning and etching a polysilicon.

17. The method of claim 14, wherein a width of a remaining portion of the insulator defines a spacing between the emitter and the raised extrinsic base.

18. The method of claim 14, wherein the extrinsic base layer is non-planar.

19. The method of claim 14, wherein the raised extrinsic base layer comprises one of: a polysilicon and single crystalline silicon.

20. The method of claim 14, wherein the conductor comprises single crystalline silicon.